Code No. 11249/N/S

FACULTY OF ENGINEERING

B.E. (I.T.) 4/4 I - Semester (New)(Suppl.) Examination, May / June 2019

Subject : VLSI Design

Time : 3 Hours | Max. Marks: 75

Note: Answer all questions from Part-A & any five questions from Part-B.

PART – A (25 Marks)

1	What is Moore€s law?	(2)
2	Draw the stick diagram of NOT gate.	(3)
3	What are blocking and non blocking statements in verilog?	(3)
4	Explain scaling concept of MOSFET.	(2)
5	Describe threshold voltage in MOSFET.	(2)
6	Design Y=A(B+C) using CMOS logic.	(3)
7	Explain charge leakage in clocked CMOS logic.	(2)
8	Describe fanout and input capacitance in CMOS inverter.	(3)
9	Define pass transistor logic.	(2)
10	Explain multiple rung ladder network.	(3)

PART – B (50 Marks)

11	(a) Draw transmission gate using 4x1 mux.	(5)
	(b) Draw RC model of FET with MOS capacitances.	(5)
12	Explain the fabrication of CMOS process.	(10)
13	(a) Draw the layout of transmission gate and non inverting buffer.	(7)
	(b) Draw the RC switch model of CMOS inverter.	(3)
14	(a) Explain read and write operation of 4T SRAM.	(7)
	(b) Explain IT dynamic RAM.	(3)
15	(a) Explain different kinds of modelling techniques in verilog.	(7)
	(b) Explain master slave D flipflop operation.	(3)
16	(a) Design complementary pass Transistor logic using AND/NAND gates.	(5)
	(b) Describe rise time and fall time in CMOS inverter.	(5)
17	Write short notes on:	
	(a) latch up condition	(5)
	(b) Crosstalk	(5)

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